ACADEMIA JOURNALS
OPUS PRO SCIENTIA ET STUDIUM

SAN ANTONIO, TX
INFO@ACADEMIAJOURNALS.COM
ACADEMIAJOURNALS.COM

15 septiembre 2020

AUTORES: Marcos Alberto Camarena Rivera
Dr. Noé Amir Rodríguez Olivares

ARTÍCULO: **Alternative test flow for the electrical validation of USB 2.0 receiver circuits**

ARTÍCULO Núm: T183

Estimados autores,

Con agrado les informamos que, con fecha de hoy, el artículo arriba citado ha sido aprobado para su presentación en el Congreso International de Investigación Academia Journals Tabasco 2020. El congreso tendrá lugar los días 23 al 25 de septiembre del año 2020, en Villahermosa, Tabasco, México.

El artículo será incluido en las publicaciones del congreso, que incluyen modalidades ISBN, ISSN, e indización en *Fuente Académica Plus* de EBSCOHost.

Le rogamos que utilice su número de artículo en toda correspondencia con Academia Journals.

Saludos cordiales.

Dr. Rafael Moras, P.E.
Editor
Academia Journals
Info@academiajournals.com

ACADEMIA JOURNALS

OPUS PRO SCIENTIA ET STUDIUM

CERTIFICADO

otorgado a

Marcos Alberto Camarena Rivera
Noé Amir Rodríguez Olivares

por su artículo intitulado

Alternative Test Flow for the Electrical Validation of USB 2.0 Receiver Circuits

(Artículo No. T183)

El congreso fue organizado en colaboración con la División Académica de Ciencias Biológicas de la Universidad Juárez Autónoma de Tabasco, México. La ponencia de este artículo fue presentada en el congreso desarrollado los días 23 al 25 de septiembre de 2020. El artículo fue publicado en las siguientes modalidades: (1) en el portal de Internet *AcademiaJournals.com*, con ISSN 1946-5351 online, Vol. 12, No. 6, 2020 e indexación en la base de datos Fuente Académica Plus de EBSCOHOST, Massachusetts, Estados Unidos y (2) en el libro electrónico intitulado *Diseminación de Resultados de Investigación Universitaria - Tabasco 2020,* mismo que cuenta con ISBN 978-1-939982-61-2 online.

CONGRESO DE INVESTIGACIÓN ACADEMIA JOURNALS

Dr. Rafael Moras, P.E.
Director, Academia Journals

T183

Alternative Test Flow for the Electrical Validation of USB 2.0 Receiver Circuits

Marcos Alberto Camarena Rivera[1][2],
Noé Amir Rodríguez Olivares[3][4]

***Abstract*— Electrical validation of USB 2.0 High-Speed receiver, used for multiple generations of Intel products, has been relying on the compliance sensitivity test method performed in Device Mode, as defined from USB Implementers Forum. This paper presents a new test strategy to develop a more simplified and convenient test method performed on Host Mode. A new test emerged as a better alternative to eliminate the dependencies from Windows OS and the driver for the extensible host controller and a device controller to enable Device Mode and achieve dual-role support. Deployed during 2019 at Intel Guadalajara Design Center, it dramatically reduced the required time to start validation activities of the receiver circuit during the early stages of products. The new method is intended to be the product of record solution for USB 2.0 receiver circuit for Intel post-silicon electrical validation across business units and product segments.**

***Keywords*— USB 2.0, electrical validation, receiver sensitivity, host mode, squelch**

Introduction

As defined by USB Implementers Forum (USB-IF, 2000), USB 2.0 is a half-duplex unidirectional serial data interface that transfers signal and power over a four wired scheme, two differential lines for data (DP and DM) and two lines for power (+5V and GND). It supports High-Speed (HS) data rates of 480 Mbps and is fully compatible with USB1.x for Full-Speed and Low-Speed modes.

One of the most useful functionalities of USB2 according to Axelson (Axelson, 2009) resides on the ability for devices to be hot-swappable by allowing them to be connected and disconnected at any time without the need to reboot the Host computer. Aligned with USB-IF (USB-IF, 2012) this capability is extended when connecting two host computers through a USB2 port that is Device Mode capable, usually a Type-C connector; a negotiation process is performed within the OS and USB2 controller drivers involved in order to define which one of the computers performs the role of Host and which one behaves as the device. This functionality is known as USB2 Device Mode and is mainly used to enable direct point to point transfer of data.

USB2 owners in post-silicon electrical validation have seen that one of the main challenges during validation activities is related to the enabling of USB2 Device Mode within Windows OS, which requires to update the drivers for the extensible host controller and a device controller to achieve dual-role support, in order to perform compliance test for Receiver Sensitivity, as defined by the USB-IF; validation teams usually work with prototype versions of microprocessors that are linked to earlier versions of Windows OS and USB controller drivers that are not mature enough to fulfill the needs required for compliance testing of USB2 receiver.

The new test method has helped optimize the overall validation strategy by enabling new test capabilities in Host Mode for receiver circuit during early stages of products and eliminating dependencies of Windows OS and USB2 controller drivers that are inherent to Device Mode. As an additional benefit, it has helped to assure the quality of products, having a direct and positive impact in making sure bugs are being found and fixed towards zero customer escapes.

Method description

Summary of the investigation challenges

During 2019 a cross-functional team from USB2 Electrical Validation and Circuit Design took on a joint goal to enable the functionality of USB2 receiver circuit in Host Mode without the need to reach Windows OS. Activities were undertaken for the on-going program being validated at the time with the intention to later deploy a new test method for the Signal Integrity Validation (SIV) of the USB2 receiver circuit across programs and segments.

[1] Marcos Alberto Camarena Rivera. Student of the Master's Program "Sistemas Inteligentes Multimedia" at Posgrado CIATEQ A.C. mcamarena27@yahoo.com.mx **(corresponding author)**
[2] Professional in Electrical Validation at "Intel Tecnología de México S.A de C.V". marcos.camarena@intel.com
[3] Noé Amir Rodríguez Olivares is a Thesis Advisor at Posgrado CIATEQ A.C.
[4] Professor at "Centro de Ingeniería y Desarrollo Industrial (CIDESI)". noe.amir@gmail.com

Basics of USB2 Electrical Validation

Electrical Validation (EV) ensures the compliance of signal integrity and provides tuning of an analog interface over process, voltage and temperature conditions. The impact of platform trace lengths and topologies are also considered. Measurements of SIV are becoming more important because they enable the manufacturers to certify the electrical performance of USB2 in their products and permits them to use the official USB 2.0 High Speed (HS) logo after they pass the tests for the compliance certification program.

The performance of USB2 greatly depends on the electrical parameters obtained from the analog circuits for the transmission and reception of data. USB-IF defines the mandatory electrical tests for certification of a USB2 product. The compliance application for USB2 Electrical testing from Keysight (Keysight, 2019) aligned with USB-IF (USB-IF, 2000) lists the set of tests in HS for Host Mode and Device Mode as shown in Table 1.

Host Mode Tests	Device Mode Tests
Host HS Signal Quality	Device HS Signal Quality
Host Controller Packet Parameters	Device Packet Parameters
Host CHIRP Timing	Device CHIRP Timing
Host Suspend / Resume Timing	Device Suspend / Resume / Reset Timing
Host Test J/K SE0_NAK	Device Test J/K SE0_NAK
	Device Receiver Sensitivity

Table 1. Compliance tests for USB2 HS Host Mode and Device Mode.

From Table 1 we can identify that Receiver Sensitivity test is defined only for Device Mode capable products, or in other words, Receiver Sensitivity test validates a circuit that has not been covered in the tests for Host Mode.

Basics of USB2 receiver buffer

On a high-level, the USB2 receiver buffer contains analog circuit blocks to monitor voltage changes in the differential data lanes in order to determine if a signal is considered noise (Squelch) or if a valid signal has been received (Unsquelch). According to USB-IF (USB-IF, 2012) these conditions are defined by the following tests:

- Test ID EL_16 (Receiver sensitivity test @ Squelch): A High-Speed (HS) capable device may not become too sensitive and should not answer packets below 100mV.
- Test ID EL_17 (Receiver sensitivity test @ Unsquelch): A HS product should be capable of reliably answering all packets at voltage levels above 200 mV.

USB2 Receiver Sensitivity test

The USB-IF has defined a set of measures of acceptance for the electrical parameters for each operation mode. Test equipment vendors have developed software licenses for their oscilloscopes that provide step by step instructions to perform the complete set of USB2 compliance tests.

There are a couple of shortcomings of the Receiver Sensitivity test that impact the validation of the receiver circuit, resulting from dependencies on Windows OS and a driver for the USB controller to achieve Dual-Role support. Unfortunately, the test requirements related to Windows OS and Device mode driver can't be guaranteed during the early stages of microprocessor products, which prevents the USB2 Receiver Sensitivity test from being performed. Many factors will influence the deliverables of Windows OS and USB controller drivers. According to Keysight, the compliance test app for electrical testing of USB2 (Keysight, 2019) includes the test equipment requirements for the Receiver Sensitivity test, as indicated in Table 2.

Quantity	Item
1	Digital pattern generator
2	Transition time converters
1	Oscilloscope
1	Differential probe
1	Receiver sensitivity test fixture with 4" USB cable
1	5V power supply
2	50-ohm coaxial cable
1	5m USB 2.0 HS cable
1	Host test bed computer

Table 2. Test equipment for Receiver Sensitivity test.

Figure 1 shows the test setup for Receiver Sensitivity, where the Test bed computer will initiate the USB2 controller in Device Mode for the device under test (DUT), the Pulse generator will emulate the input packets from the Host controller and the Oscilloscope will measure the Squelch and Unsquelch voltage thresholds for the Validation platform.

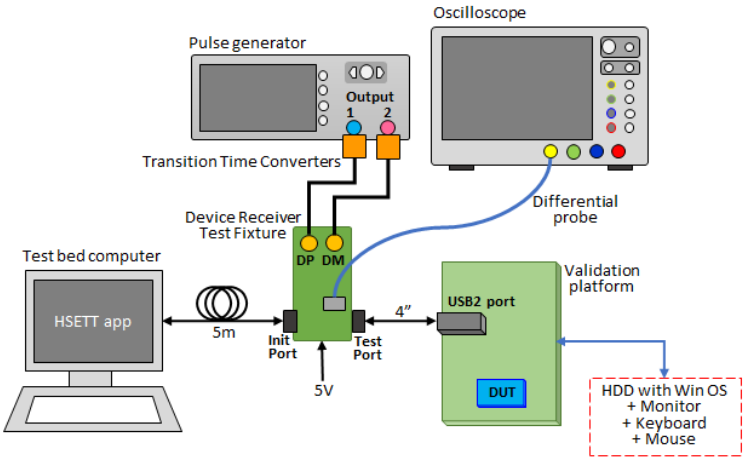

Figure 1. Test setup for Receiver Sensitivity test.

Following the Keysight automation process for USB2 testing (Keysight, 2019), the USB2 Device Mode functionality is represented by the connections of the Test bed computer with the Validation platform through the Test Fixture, the Test bed computer will act as the Host and the Validation platform will act as the Device in the bus. After the connections are completed and the USB controller driver has been updated in the Windows OS in the Device, the Host should detect the Validation Platform as "Windows Dual-Role" under the Device Manager settings. Only after that, the test can be executed.

In order to run the test per instructions from Keysight USB2 compliance app (Keysight, 2019), the steps require to enumerate the bus on the High-Speed Electrical Test Tool (HSETT) application under Device Test menu, then select and execute the test mode for TEST_SE0_NAK.

USB2 alternative test for Receiver AC Squelch

There are limitations with Receiver Sensitivity test, performed at system level in which USB controller, Windows OS and USB driver are all involved. In this scenario, it's difficult to achieve the enabling of the signal because of the need to reach dual role support for the USB controller in the Validation platform.

The challenge is to find an alternative approach in which the same electrical parameters for Squelch and Unsquelch can be verified so that SIV of receiver circuit is fully autonomous and unblocked from external dependencies. The alternative test flow proposed in this investigation is called Receiver AC Squelch Test and the simplified test setup is shown in Figure 2.

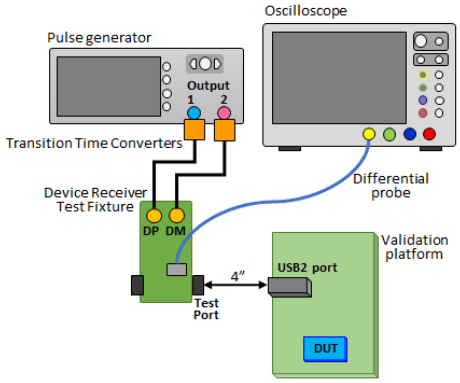

Figure 2. Simplified test setup for Receiver AC Squelch test.

The Receiver AC Squelch test consists of two sequences. In the first one, a sweep of the signal amplitude from a low to a high value is performed to validate and obtain the Squelch voltage level. This voltage level will be identified by the state change of a bit in a USB2-PHY register. In the second sequence, the Unsquelch functionality level will be validated by performing a sweep of the signal amplitude from high to a low value, using the state change of the same register. Figure 3 shows the block diagram sequence of the test flow.

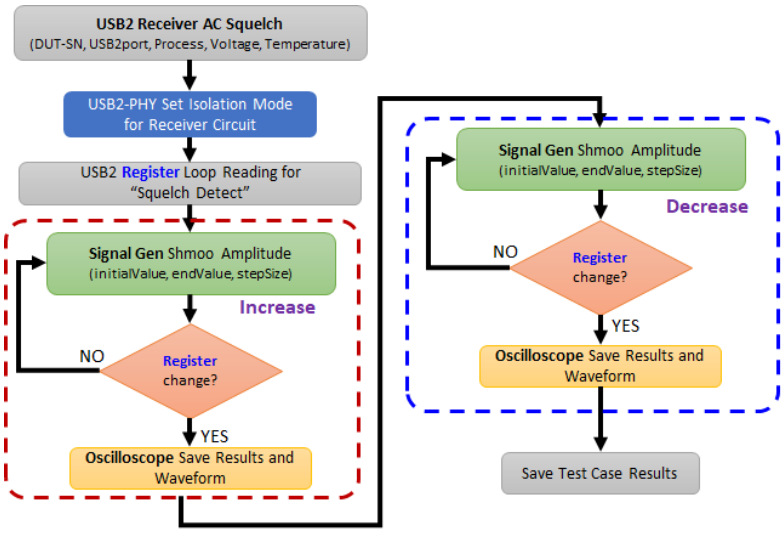

Figure 3. Test flow for Receiver AC Squelch test.

In Figure 3, the content blocks identified as "USB2-PHY Set Isolation Mode for Receiver Circuit" and "USB2 Register Loop Reading for Squelch Detect" correspond to an specific Design for Testability (DFx) of the USB2-PHY within Intel microprocessors and represent Intel Confidential Information, therefore no additional details can be provided. The blocks contained inside the dotted red square correspond to an increase of the voltage amplitude of the input signal; these blocks are used to validate the Squelch voltage threshold. The second sequence for Unsquelch functionality, where the input signal will be decreased, corresponds to the blocks contained inside the blue dotted square.

Final Comments

There are many advantages of Receiver AC Squelch test. This approach is well suited for electrical testing of USB2 receiver as it directly communicates with the USB2-PHY and validates the Squelch and Unsquelch voltage levels using the same specification limits for the Receiver Sensitivity test.

Summary of results

The effort to enable the signal content required for performing Receiver Sensitivity compliance test is higher and takes long time due to external dependencies. The benefit of the alternative test for Receiver AC Squelch is that the execution can be performed right out of the box during early stages of validation programs. Due to the limited time that validation teams have to perform their activities, this approach is worthwhile and represents a tangible benefit. Receiver AC Squelch test was initially used in four generations of microprocessor products for EV in a business unit (BU) for a product segment; later it was adopted across the rest of BU's and segments, both locally and overseas.

Conclusions

Receiver AC Squelch test delivers a high level of functionality for the USB2 receiver, based on the enabling of the circuit from the USB2-PHY, while avoiding the complexity of the USB controller driver and its integration with Windows OS, along with exploiting a simpler test setup configuration. A key point about the new approach is that it is a simple and integral solution in which the signal content enabling is embedded in the test flow.

This test flow has the potential to become the product of record solution for the SIV of USB2 receiver for EV post-silicon activities. It is ideal for validating early versions of the programs where Windows OS and USB controller drivers are still in development. It also helps to improve the confidence of the EV team to produce a robust risk assessment during the required milestones of the validation life cycle of the product.

References

USB-IF. “Universal Serial Bus Electrical Test Specification revision 2.0”. 2000. Internet address: https://www.usb.org/documents

Axelson, J. “USB Complete. The Developer’s Guide”. Fourth Edition. Lakeview Research. 2009.

USB-IF. “On-The-Go and Embedded Host Supplement to the USB revision 2.0 Specification”. 2012.
Internet address: https://www.usb.org/documents

Keysight. “D9010USBC USB 2.0 Compliance Test Application. Notes on Electrical Testing”. Version 4.01.0000. December 2019.
Internet address: https://www.keysight.com/